CLAIMS

What is claimed is:

1. A structure of nonvolatile memory array, comprising:

a substrate;

a plurality of isolation region in said substrate;

a buried conductive region between said isolation regions, wherein said buried conductive region is perpendicular to said isolation region; and

a plurality of gate structure on said substrate.

2. The structure according to claim 1, wherein said isolation region is shallow trench isolation.

3. The structure according to claim 1, wherein a depth of said buried conductive region is less than a depth of said isolation region.

4. The structure according to claim 1, wherein said gate structure comprises at least a polysilicon layer.

5. The structure according to claim 1, further comprising a plurality of contact on said substrate.

6. The structure according to claim 1, wherein said buried conductive region is a source line.

7. The structure according to claim 1, further comprising a

plurality of drain region in said substrate.

8. The structure according to claim 1, wherein said buried conductive region is on a surface of said substrate, such that said buried conductive region is not under said isolation region.

9. A structure of nonvolatile memory array, comprising:

a substrate;

a plurality of isolation region in said substrate;

a plurality of gate structure on said substrate;

a buried source line between said isolation regions, wherein said buried source line is perpendicular to said isolation regions; and

a plurality of drain region in said substrate.

10. The structure according to claim 9, wherein said isolation region is shallow trench isolation.

11. The structure according to claim 9, wherein a depth of said buried source line is less than a depth of said isolation region.

12. The structure according to claim 9, wherein said gate structure comprises at least a polysilicon layer.

13. The structure according to claim 9, further comprising a plurality of contact in said substrate.

14. A source line structure of a nonvolatile memory array, comprising:

a substrate;

a plurality of isolation region in said substrate; and

a buried conductive region between said isolation regions, wherein said buried conductive region is perpendicular to said isolation regions.

15. The structure according to claim 14, wherein said buried conductive region is on a surface of said substrate.

16. The structure according to claim 14, wherein a depth of said buried conductive region is less than a depth of said isolation region.

17. The structure according to claim 14, wherein said isolation region is shallow trench isolation (STI).

18. The structure according to claim 14, further comprising a plurality of gate structure on said substrate.

19. The structure according to claim 18, wherein said gate structure comprises at least a polysilicon layer.

20. The structure according to claim 14, wherein said buried conductive region is on a surface of said substrate, such that said conductive region is not under said isolation regions.